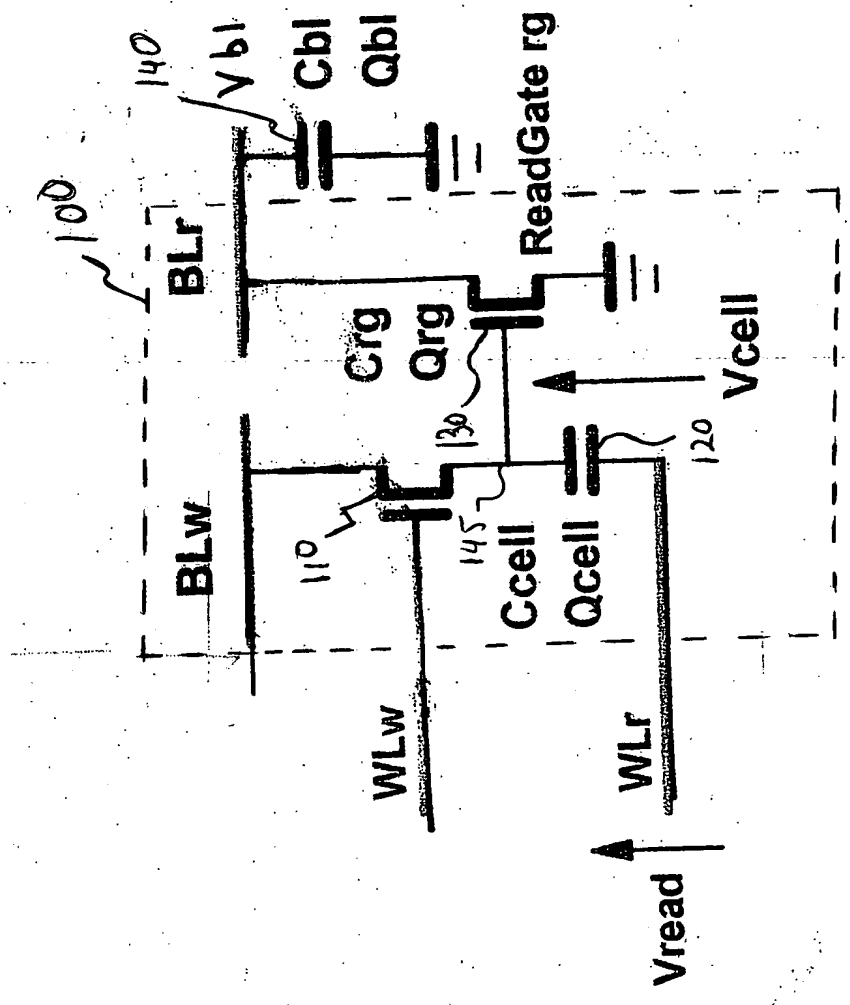
100
140
Vbl
Cbl
Qbl
BLr
ReadGate rg
Crg
Qrg
130
Vcell
120
BLW
110
145
Ccell
Qcell
WLw
WLr
Vread

FIG. 1

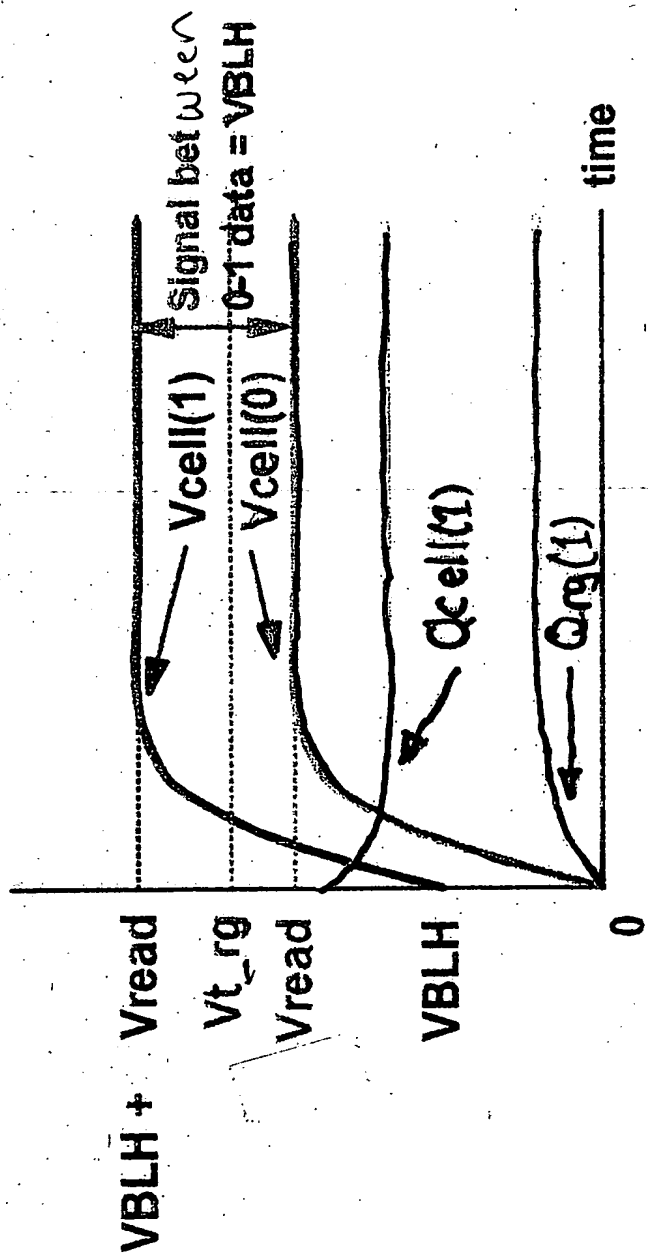
VBLH +
Vread
Vt_rg
Vread
VBLH
0
time
Vcell(1)
Signal between
0-1 data = VBLH
Vcell(0)
Qcell(1)
Qrg(1)

FIG. 2

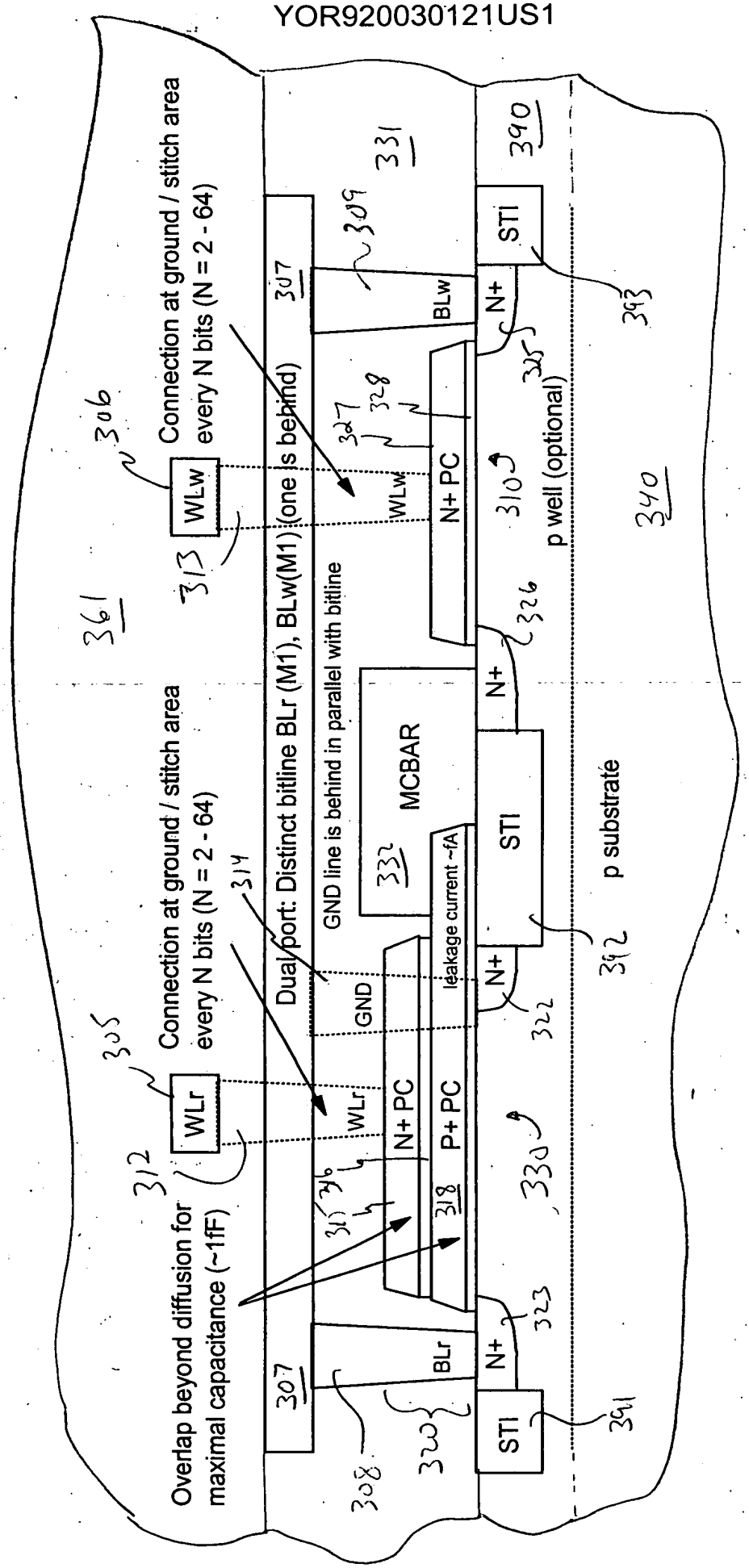
300
Connection at ground / stitch area every N bits (N = 2 - 64)
Dual port: Distinct bitline BLr (M1), BLw(M1) (one is behind)
GND line is behind in parallel with bitline
Connection at ground / stitch area every N bits (N = 2 - 64)
Overlap beyond diffusion for maximal capacitance (~1fF)
WLw
WLr
BLw
BLr
GND
MCBAR
leakage current ~fA
N+ PC
P+ PC
N+
STI
p well (optional)
p substrate
306
307
308
309
310
311
312
313
314
318
320
322
323
325
326
327
328
330
331
332
340
341
342
343
361
390

FIG. 3A

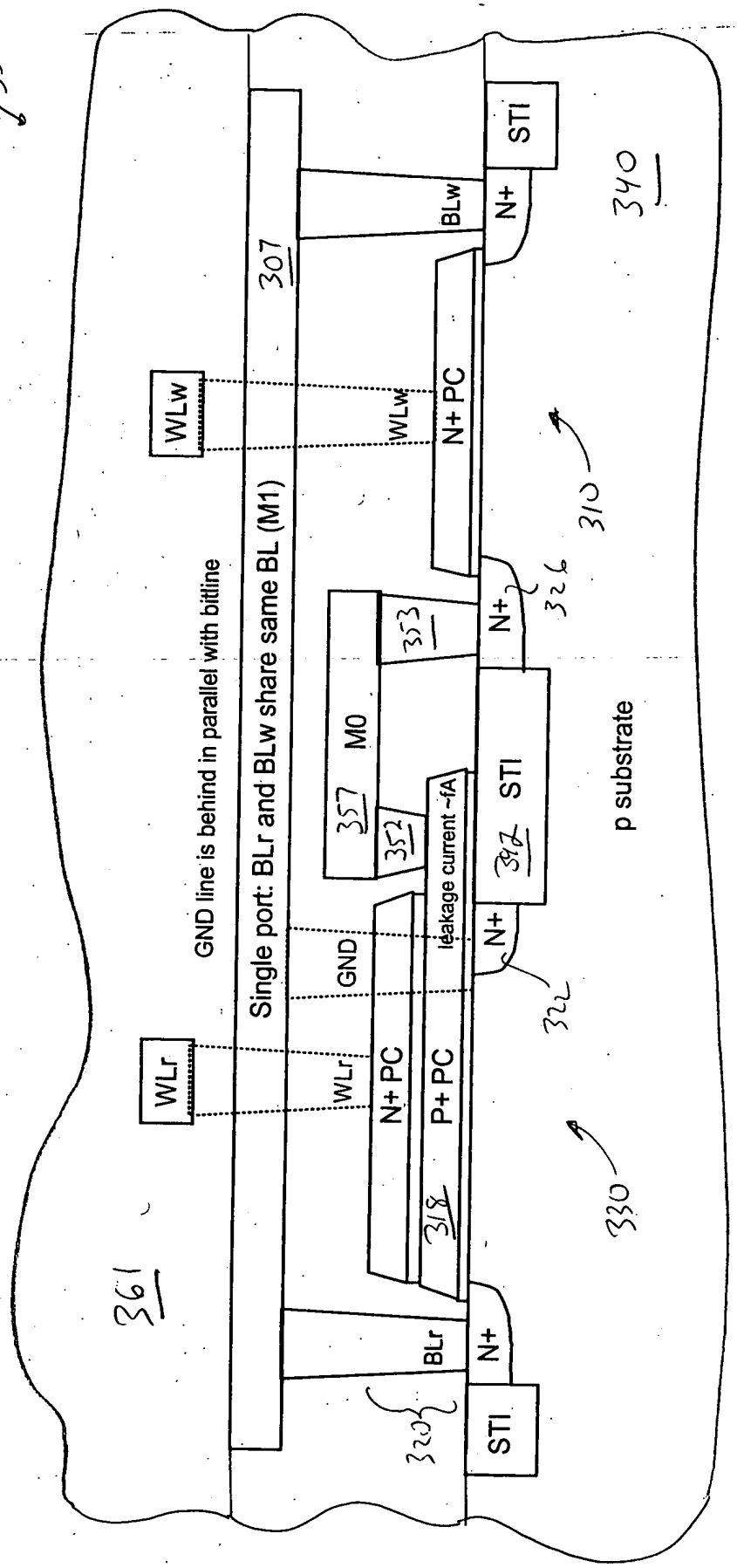
350
WLw
WLr
GND line is behind in parallel with bitline
Single port: BLr and BLw share same BL (M1)
307
WLw
WLr
GND
BLw
BLr
N+ PC
P+ PC
N+
STI
M0
leakage current ~fA
p substrate
340
310
330
361
320
326
322
318
352
353
357
382

FIG. 3B

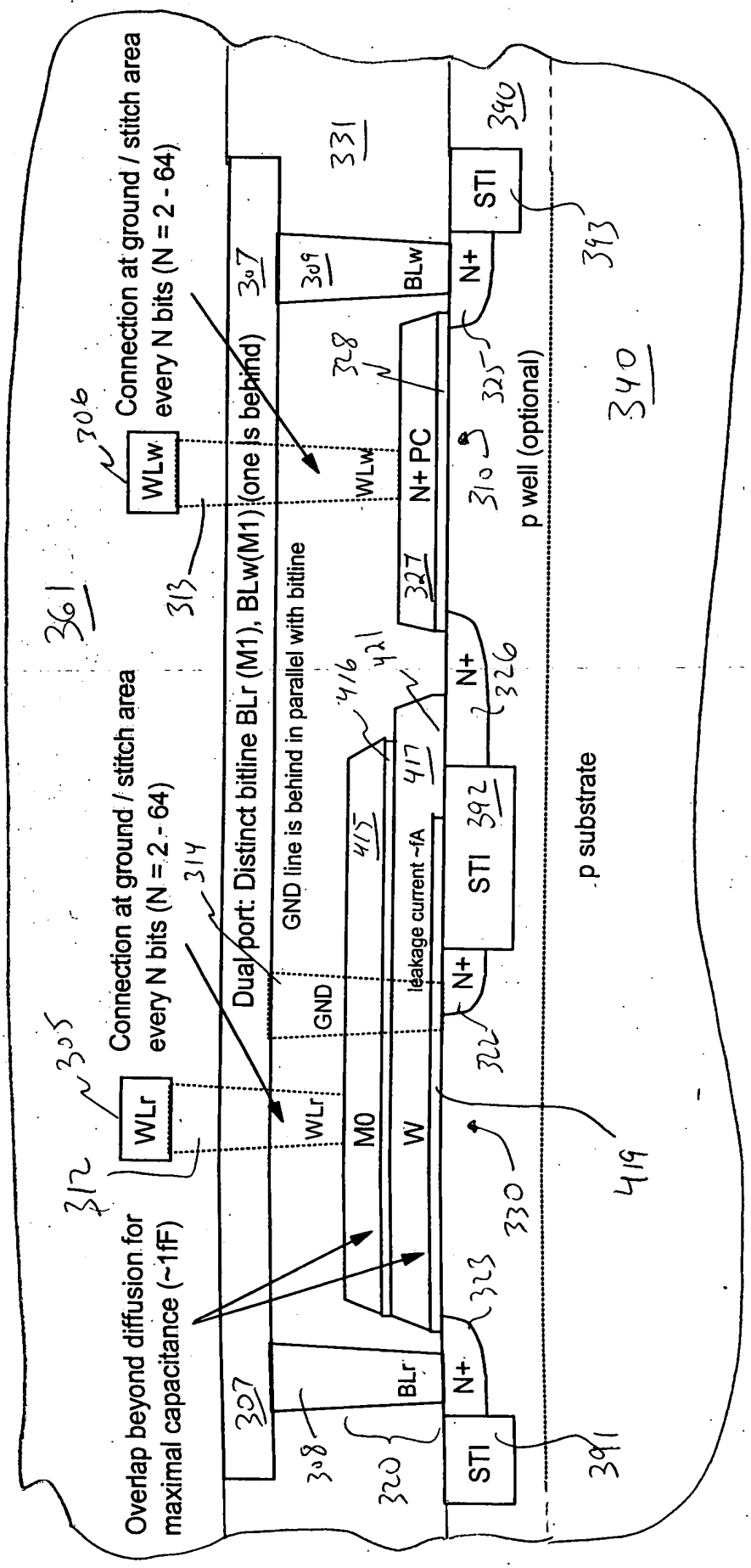
400
Connection at ground / stitch area every N bits (N = 2 - 64)
WLw
306
Dual port: Distinct bitline BLr (M1), BLw(M1) (one is behind)
307
309
BLw
331
STI
340
313
328
WLw
N+ PC
327
N+
325
310
p well (optional)
340
393
361
GND line is behind in parallel with bitline
416
421
415
417
leakage current ~fA
N+
326
STI
392
N+
322
Connection at ground / stitch area every N bits (N = 2 - 64)
305
WLr
314
WLr
MO
W
330
312
Overlap beyond diffusion for maximal capacitance (~1fF)
307
308
BLr
320
323
N+
STI
391
p substrate
419

FIG. 4A

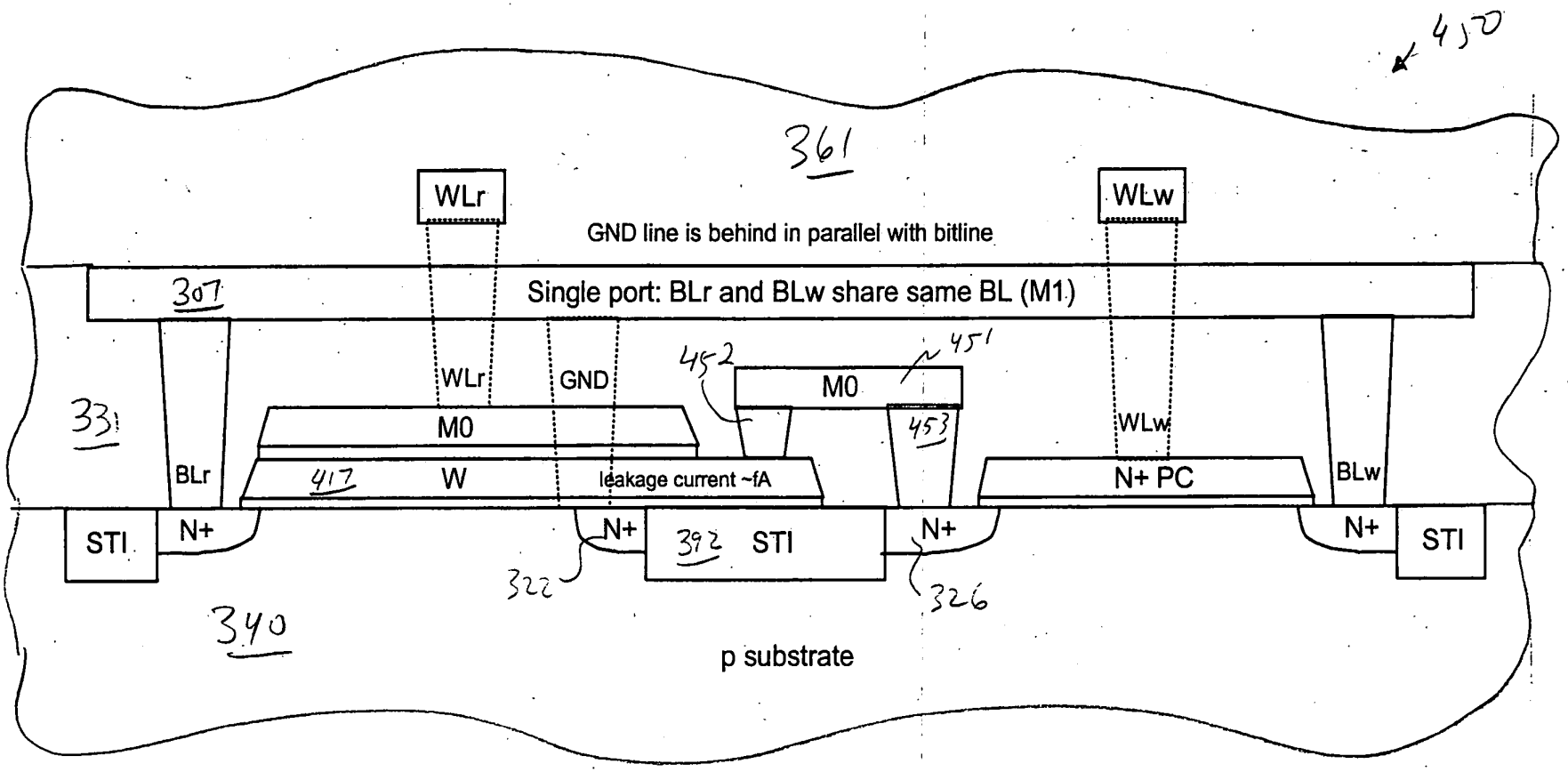
450
361
WLr
WLw
GND line is behind in parallel with bitline
307
Single port: BLr and BLw share same BL (M1)
331
WLr
GND
452
M0
451
M0
453
WLw
BLr
417
W
leakage current ~fA
N+ PC
BLw
STI
N+
N+
392
STI
N+
N+
STI
322
326
340
p substrate

FIG. 4B

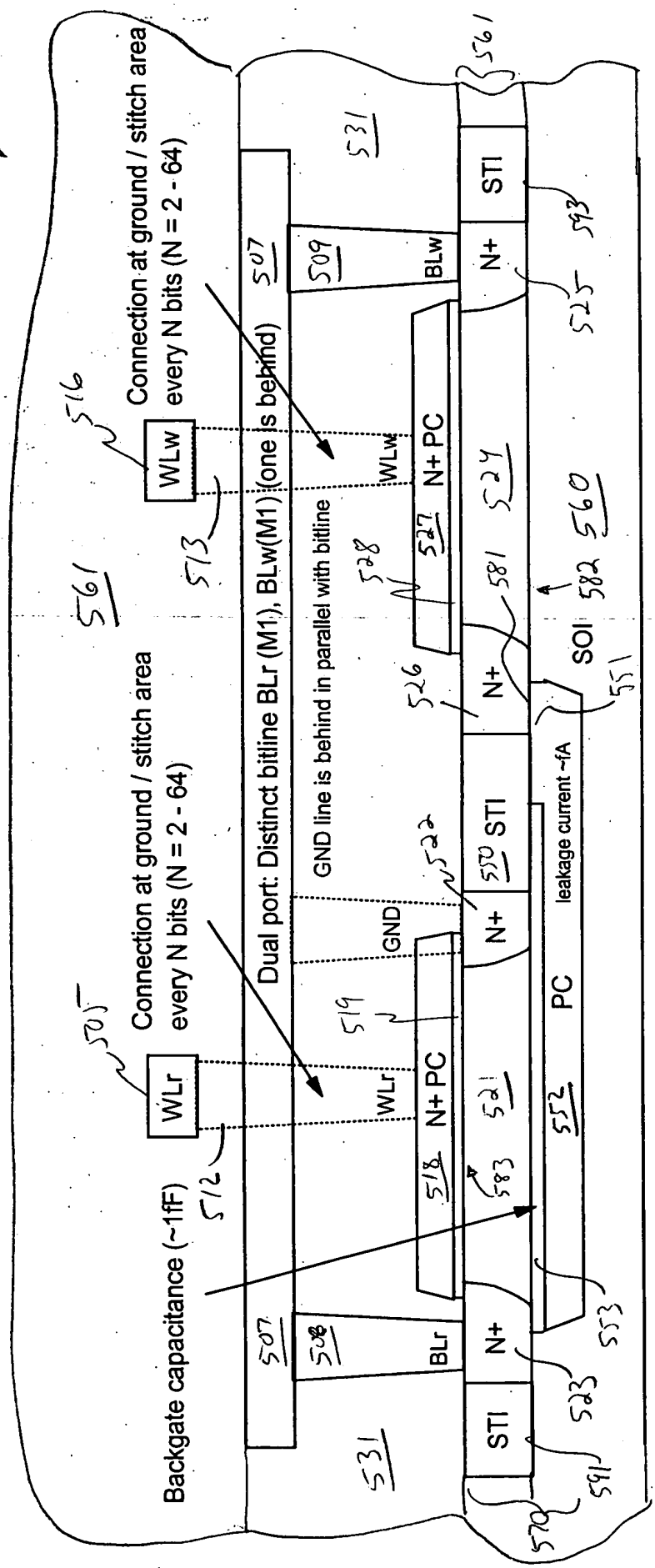
500
561
516
Connection at ground / stitch area every N bits (N = 2 - 64)
WLw
513
WLw
Dual port: Distinct bitline BLr (M1), BLw(M1) (one is behind)
507
509
BLw
531
STI
N+
525
N+ PC
527
528
581
524
526
N+
SOI
582
560
551
510
GND line is behind in parallel with bitline
GND
522
570
STI
N+
519
WLr
WLr
N+ PC
521
505
Connection at ground / stitch area every N bits (N = 2 - 64)
WLr
512
Backgate capacitance (~1fF)
518
583
PC
leakage current ~fA
552
530
507
508
BLr
N+
553
531
STI
523
591
570

FIG. 5A

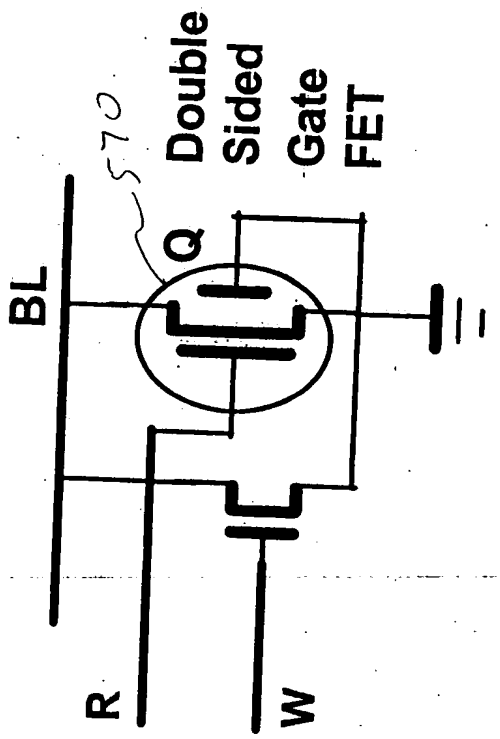
BL
570
Double
Sided
Gate
FET
Q
R
W

FIG. 5C

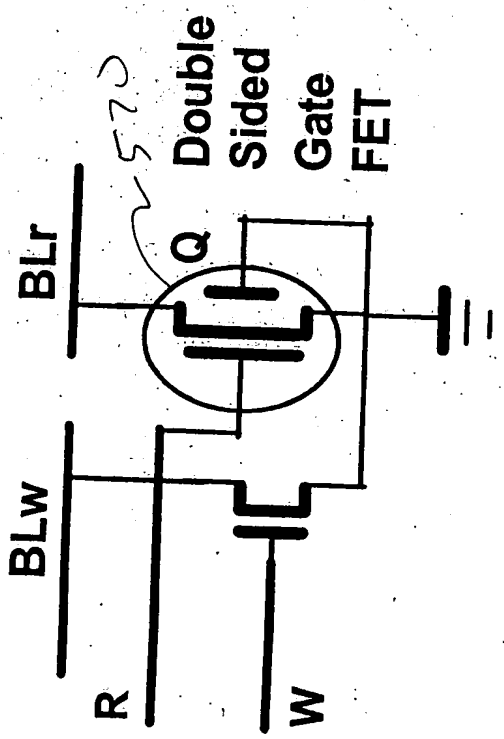
BLr
570
Double
Sided
Gate
FET
Q
BLw
R
W

FIG. 5B

Double Gate	VBLH	VWLw	VTw	VWLr	VTr	Vsrc	Vcell store, read	VBL	Vg_leak_read Vcellmax - (Vsrc + Vt)
p+, n+	0.8	-0.5~0.8	0.5	-0.8~0~0.8	1.2	0	0 ~ 0.8, 0.6 ~ 1.4	0 ~ 0.8	0.8 - (0+1.2) = -0.4
w, n+	0.5	-0.5~0.8	0.5	-0.5~0~0.8	0.8	0	0 ~ 0.7, 0.6 ~ 1.3	0 ~ 0.5	0.7 - (0+0.8) = -0.1
w, n+	0.5	-0.5~1.0	0.5	0 ~ 1.0	0.8	0	0 ~ 0.4, 0.7 ~ 1.1	0 ~ 0.5	0.4 - (0+0.8) = -0.4
p+, n+	0.5	-0.5~1.0	0.5	0 ~ 1.0	1.2	-0.5	0 ~ 0.4, 0.7 ~ 1.1	-0.x~0.5	0.4 - (-0.5+1.2) = -0.3
p+, n+	1.0	0~1.5	0.5	0 ~ 1.0	1.2	0	0.5~0.9, 1.2~1.6	0.x~ 1.0	0.9 - (0+1.2) = -0.3
p+, n+	0.4	0~1.0	0.5	0 ~ 1.0	0.6	0	0 ~ 0.4, 0.7 ~ 1.1	0 ~ 0.4	0.4 - (0+0.6) = -0.2

FIG. 6

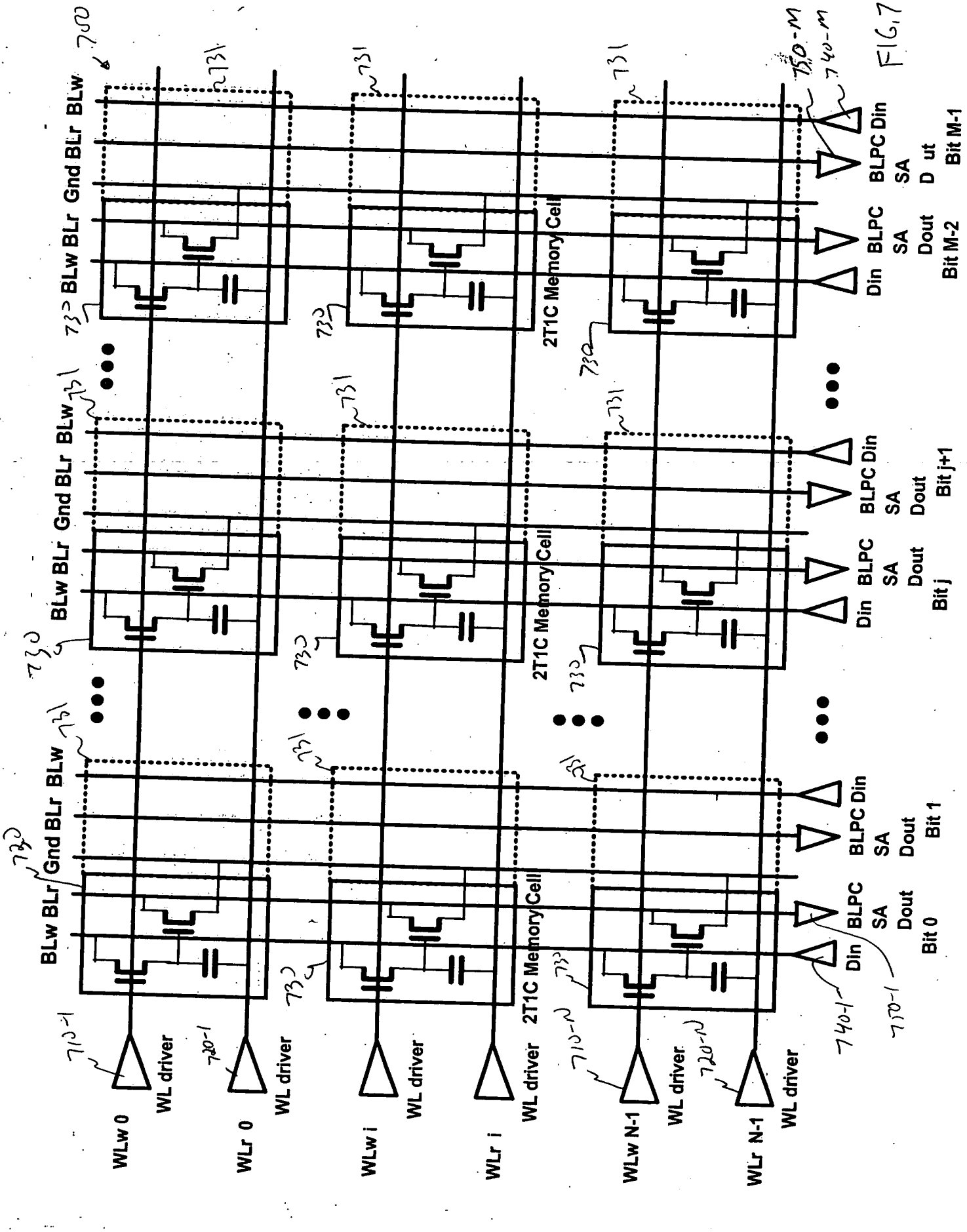
BLw BLr Gnd BLr BLw
WLw 0
WL driver
WLr 0
WLw i
WLr i
WLw N-1
WLr N-1
2T1C Memory Cell
Din BLPC SA Dout
BLPC Din SA Dout
Bit 0
Bit 1
Bit j
Bit j+1
Bit M-2
Bit M-1
D ut

FIG. 7

	Traditional 1T1C Cell	NDR 2T1C Cell	NDR 2T1C Cell (with write boost)
BLWrite	VBLH	VBLH	VBLH
Vcell_i(0,1)	0, VBLH	0, VBLH	0, VBLH + VB
Vcell_f(0,1)	0, VBLH Tr (< VBLH) Tr = Ccell/(Ccell+Cbl)	bVread, VBLH + bVread b = Ccell/(Ccell+Crg)	bVread, VBLH + VB + bVread b = Ccell/(Ccell+Crg)
Gain = (Vcell_f(0,1) / Vcell_i(0,1))	Ccell/(Ccell + Cbl) << 1, typically 0.2	1	1 Gain (over VBLH) = 1 + VB / VBLH ~ 2

FIG. 8